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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,395	01/20/2004	Tom E. Burton	42P8329D2	3296

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EXAMINER	
PASIA, REDENTOR M	

ART UNIT	PAPER NUMBER
2616	

MAIL DATE	DELIVERY MODE
06/13/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/761,395	BURTON ET AL.	
	Examiner	Art Unit	
	REDENTOR M. PASIA	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *11 March 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on March 11, 2008 has been entered. No claims were amended. No claims were cancelled. No claims have been added. Claims 19 and 20 are still pending in this application, with claim 19 being independent.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vogel (US 6,839,352 B1; hereinafter Vogel) in view of Richards et al. (US 6,801,535 B1; hereinafter Richards).

As to claim 19, Vogel shows a device (Figure 3; device 30) comprising: a first circuitry to generate a packet header based on payload data received from a micro-engine or from a memory controller (Figure 3, single-chip SONET physical layer device 30; Figure 4; col. 5, lines 31-42; col. 7, lines 34-48; interface block 42 then generates the header fields 12 for each of the ATM cells 10 based on the header field extracted from the PPP payload field.), the first circuitry comprising: second circuitry to receive packet data from the memory controller or the micro-engine, and to store the packet data in the first-in-first-out circuitry (Figure 3; col. 5, lines, 57-64;

In a standard ATM mode, ATM cells are sequentially received from an ATM Segmentation And Reassembly (SAR) processor or cell processor (not shown), for example, through UTOPIA bus interface port 34. Enhanced UTOPIA interface block 42 collects the received ATM cells in an array of storage elements, such as a stack of FIFOs. Once collected, the ATM cells are filtered and buffered in a known manner; col. 7, lines 10-11).

However, Malladi does not show a third circuitry to track a start lane in the FIFO circuitry indicating a start of free space in FIFO circuitry, and to determine a starting lane for packet payload such that the alignment of payload data matches the start lane in the FIFO circuitry.

Richards shows a circuitry (processor 12) to track a start lane in the FIFO circuitry indicating a start of free space in FIFO circuitry (figure 10), and to determine a starting lane for packet payload such that the alignment of payload data matches the start lane in the FIFO circuitry (figures 8 -11; col. 3, lines 36-60; col. 10 lines 19-55). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device of Vogel by having the memory management of Richards as discussed above in order to have proper memory management and data transmission.

As to claim 20, modified Vogel shows a logic to synchronize receipt of the packet header from the micro-engine and the packet payload from the memory controller (Richards: Figure 8-11; col. 3, lines 36-60; col. 10, lines 19-55), to store the packet header in the FIFO circuitry (Vogel: Figure 3; col. 5, lines, 57-64; In a standard ATM mode, ATM cells are sequentially received from an ATM Segmentation And Reassembly (SAR) processor or cell processor (not shown), for example, through UTOPIA bus interface port 34. Enhanced UTOPIA interface block

42 collects the received ATM cells in an array of storage elements, such as a stack of FIFOs. Once collected, the ATM cells are filtered and buffered in a known manner; col. 7, lines 10-11), and to transfer the packet header and packet payload data from the FIFO circuitry to a destination specified in the packet header (Figure 1; VPI, VCI fields; Figure 2; address field; Figure 5-6; col. 8, lines 23-64; shows the transmission modes of the device.).

Response to Arguments

4. Applicant's arguments filed March 11, 2008 have been fully considered but they are not persuasive.

As stated in the Applicant's Arguments/Remarks pages 3-5, Applicant traverses the rejection of claims 19-20 under 35 U.S.C. §103(a) as being obvious over U.S. Patent No. 6,839,352 to Vogel (hereinafter "Vogel") in view of U.S. Patent No. 6,801,535 to Richards et al. (hereinafter "Richards").

As to claim 19, Applicant argues that Vogel in view of Richards does not teach/suggest "first circuitry to generate a packet header based on payload data received from a micro-engine or from a memory controller, the first circuitry comprising: second circuitry to receive packet data from the memory controller or the micro-engine, and to store the packet data in first-in first-out (FIFO) circuitry". Mainly, Applicant argues the Vogel in view of Richards does not disclose generating a packet header based on payload data. The Examiner respectfully disagrees with the Applicant.

As shown in the above rejection, Vogel in view of Richards discloses:

"a first circuitry to generate a packet header based on payload data received from a micro-engine or from a memory controller (Figure 3, single-chip SONET physical layer device 30; Figure 4; col. 5, lines 31-42; col. 7, lines 34-48; interface block 42 then generates the header fields 12 for each of the ATM cells 10 based on the header field extracted from the PPP payload field.), the first circuitry comprising:

second circuitry to receive packet data from the memory controller or the micro-engine, and to store the packet data in the first-in-first-out circuitry (Figure 3; col. 5, lines, 57-64; In a standard ATM mode, ATM cells are sequentially received from an ATM Segmentation And Reassembly (SAR) processor or cell processor (not shown), for example, through UTOPIA bus interface port 34. Enhanced UTOPIA interface block 42 collects the received ATM cells in an array of storage elements, such as a stack of FIFOs. Once collected, the ATM cells are filtered and buffered in a known manner; col. 7, lines 10-11)"

Referring to Figure 3 of Vogel, SONET physical layer device 30 contains various circuitries or modules (40, 42, 44, 46 48). As cited in the above rejection, SONET physical layer device 30, which has UTOPIA interface block 42, **generates the header fields for each of the ATM cells 10 based on the header field extracted from the PPP payload field** (col. 7, lines 34-48). Other parts of the citation also shows, that "PPP processing block 44 extracts the ATM cell header field from the beginning of the PPP payload field, extracts the protocol data unit from the remainder of the PPP payload field data and provides the ATM cell header and the protocol data unit to enhanced UTOPIA interface block 42. With the above given rejection, Vogel in

view of Richards shows the first circuitry (SONET physical layer device 30 containing UTOPIA interface block 42 – see Figure 3), the step to generate a packet header based on payload data received (see above citations,– emphasis on col. 7, lines 34-48) and micro-engine or memory controller (Figure 3, PPP processing block, col. 7, lines 34-48).

The Examiner has also observed, that claim language presented in claim 19 shows that the first circuitry comprises the second circuitry. However, claim language also does not show a link between, a packet header and the payload data, to the packet data (which was introduced by the second circuitry – *"second circuitry to receive packet data"*). With the above observation, The Examiner notes that the packet header and payload data is not necessarily the same as the packet data shown in the second limitation and has been treated as such.

With the above rejection and further reasoning, Vogel in view of Richards, thus, disclose "first circuitry to generate a packet header based on payload data received from a micro-engine or from a memory controller, the first circuitry comprising: second circuitry to receive packet data from the memory controller or the micro-engine, and to store the packet data in first-in first-out (FIFO) circuitry"

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Malladi et al. (US 5598541) – note abstract;

Delvaux et al. (US 6490639 B1) – note abstract;

Karlsson et al. (US 7215670 B1) – note abstract;

Lincoln et al. (US 6829240 B1) – note abstract;

Gotesman et al. (US 6097734) – note abstract;

1. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to REDENTOR M. PASIA whose telephone number is (571)272-9745. The examiner can normally be reached on M-F 7:30am to 4:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Aung Moe can be reached on (571)272-7314. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Aung S. Moe/
Supervisory Patent Examiner, Art Unit 2616

/Redentor M Pasia/
Examiner, Art Unit 2616